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(54) **Title:** SHARING IDLED PROCESSOR EXECUTION RESOURCES

(57) **Abstract:** A processor including a plurality of logical processors, and an instruction set, the instruction set including of one or more instructions which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors in response to the first logical processor being scheduled to enter an idle state.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
G06F9/38   G06F9/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/184290 A1 (OLSZEWSKI BRET RONALD ET AL) 5 December 2002 (2002-12-05) page 2, right-hand column, paragraphs 22,26 page 3, left-hand column, paragraph 28 – paragraph 29	1–28
A	"Dynamic logical partitioning in IBM eserver pSeries" IBM WHITE PAPER, 8 October 2002 (2002-10-08), pages 1-9, XP002288348 page 1, right-hand column, paragraph 2 page 2, right-hand column, paragraph 1 page 3, left-hand column, paragraph 1 – paragraph 2	1,3,5,7, 8,10, 12-15, 17-20, 22,24, 26,27

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2006	27/03/2006

Name and mailing address of the ISA	Authorized officer
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